1. Introduction

The semiconductor transistor has been one of the most remarkable inventions of all time. It has become the main component of all modern electronics. The miniaturisation trend has been very rapid, leading to ever decreasing device sizes and opening endless opportunities to realise things which were considered impossible.
To keep up with the pace of large scale integration, the idea of single electron transistors (SETs) has been conceived. The most outstanding property of SETs is the possibility to switch the device from the insulating to the conducting state by adding only one electron to the gate electrode, whereas a common MOSFET needs about 1000–10,000 electrons [1]. The Coulomb blockade or single-electron charging effect, which allows for the precise control of small numbers of electrons, provides an alternative operating principle for nanometre-scale devices. In addition, the reduction in the number of electrons in a switching transition greatly reduces circuit power dissipation, raising the possibility of even higher levels of circuit integration [2].
The present report begins with a description of Coulomb blockade, the classical theory which accounts for the switching in SETs. We also discuss the work that has been done on realising SETs and the digital building blocks like memory and logic.
Various structures have been made in which electrons are confined to small volumes in metals or semiconductors. Perhaps not surprisingly, there is a deep analogy between such confined electrons and atoms [3]. Such regions with only dimensions of 1-100 nm and containing between 1,000 to 1,000,000 nuclei are referred to as 'quantum dots', 'artificial atoms' or 'solid state atoms'[4]. Such quantum dots form the heart of the SET gates.

2. Coulomb Blockade

Single electron devices differ from conventional devices in the sense that the electronic transport is governed by quantum mechanics. Single electron devices consist of an 'island', a region containing localized electrons isolated by tunnel junctions with barriers to electron tunneling. In this section, we discuss the electron transport through such devices and how Coulomb blockade originates in these devices. We also discuss how this is brought into play in SETs. The discussion is adapted from [30].

The energy that determines the transport of electrons through a single-electron device is **Helmholtz's free energy**, F, which is defined as difference between total energy, E_Σ ,stored in the device and work done by power sources, W. The total energy stored includes all components that have to be considered when charging an island with an electron.

$$F = E_\Sigma - W \qquad (1)$$

$$E_\Sigma = E_C + \Delta E_F + E_N \qquad (2)$$

The change in Helmholtz's free energy a tunnel event causes is a measure of the probability of this tunnel event. The general fact that physical systems tend to occupy lower energy states, is apparent in electrons favouring those tunnel events which reduce the free energy.

The components of E_Σ are:

2.1 Electron Electron Interaction, E_C

An entirely classical model for electron-electron interaction is based on the electrostatic capacitive charging energy. The interaction arises from the fact, that for every additional charge *dq* which is transported to a conductor, work has to be done against the field of already present charges residing on the conductor. Charging an island with capacitance C with an electron of charge e requires

$$E_C = \frac{e^2}{2C} \qquad (3)$$

2.2 Fermi Energy, ΔE_F

Systems with sufficiently small islands are not adequately described with the above classical model alone. They exhibit a second electron-electron interaction energy, namely the change in Fermi energy, when charged with a single electron.

2.3 Quantum Confinement Energies, E_N

With decreasing island size the energy level spacing of electron states increases indirectly proportional to the square of the dot size. Taking an infinite potential well as a simple model for a quantum dot, one calculates by solving Schrödinger's equation

$$E_N = \frac{1}{2m^*}\left(\frac{hN}{2d}\right)^2 \qquad (4)$$

2.4 Work Done by Voltage Sources, W

To evaluate the available energy for a given tunnel event, the work done on the system by the power supplies has to be included, since thermodynamically the interacting islands represent an open system. The work done by the voltage sources may be written as the time integral over the power delivered to the system.

$$W = \sum_{sources} \int V(t) I(t)\, dt \qquad (5)$$

2.5 Condition for Coulomb Blockade

2.5.1 Minimum Tunnel Resistance for Single Electron Charging

The formulation of the Coulomb blockade model is only valid, if electron states are localized on islands. In a classical picture it is clear, that an electron is either on an island or not. That is the localization is implicit assumed in a classical treatment. However a more precise quantum mechanical analyses describes the number of electrons localized on an island N in terms of an average value, $\langle N \rangle$ which is not necessarily an integer. The Coulomb blockade model requires.

$$\left| N - \langle N \rangle \right|^2 \ll 1 \qquad (6)$$

Clearly, if the tunnel barriers are not present, or are insufficiently opaque, one can not speak of charging an island or localizing electrons on a quantum dot, because nothing will constrain an electron to be confined within a certain volume.

A qualitative argument is to consider the Heisenberg Energy Uncertainty of an electron

$$\Delta E \Delta t > h/4\pi \qquad (7)$$

the energy gap associated with a single electron and the characteristic time for charge fluctuations is the time constant for charging capacitance C through tunnel resistor R_T is

$$\Delta E = e^2/2C, \quad \Delta t \simeq R_T C \qquad (8)$$

Combining these two gives the condition for the tunnel resistance

$$R_T > h/2\pi e^2 = 25813\Omega \qquad (9)$$

Experimental tests have also shown this to be a necessary condition for observing single-electron charging effects [5].

2.5.2 Requirement on temperature/voltage

The thermal kinetic energy of the electron must be less than the Coulomb repulsion energy which will lead to reduction in current leading to blockade.

$$kT < E_C \qquad (10)$$

To observe the Coulomb blockade, and SET oscillations, one has to protect the very small tunnel junctions against the shunting influence of the environment. This can be done by surrounding it with thin film resistors. The special (and simplest) case of the two junction one dimensional array leads us to the device called the single electron transistor, discussed later in the report.

3. The Double Tunnel Junction

Consider two tunnel junctions in series biased with an ideal voltage source as shown in Fig. . The charges on junction one, junction two, and on the whole island can be written as

$$q_1 = C_1V_1,\ q_2 = C_2V_2,\ q = q_2 - q_1 + q_0 = -ne + q_0 \qquad (11)$$

n_1 the number of electrons that tunnelled through the first junction entering the island, n_2 the number of electrons that tunnelled through the second junction exiting the island, and n=n_1-n_2 the net number of electrons on the island.

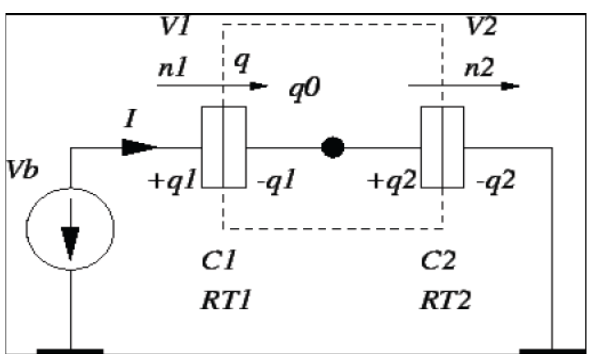


Figure 1: equivalent circuit for double tunnel junction

A background charge q_0 produces generally a non-integer charge offset. The background charge is induced by stray capacitances that are not shown in the circuit diagram Fig 1 and impurities located near the island, which are practically always present. Using (11) and

$$V_b = V_1 + V_2 \qquad (12)$$

gives

$$V_1 = \frac{C_2 V_b + ne - q_0}{C_\Sigma}, \; V_2 = \frac{C_1 V_b - ne + q_0}{C_\Sigma}, \; C_\Sigma = C_1 + C_2 \qquad (13)$$

The electrostatic energy stored in the double junction is

$$E_C = \frac{q_1^2}{2C_1} + \frac{q_2^2}{2C_2} = \frac{C_1 C_2 V_b^2 + (ne - q_0)^2}{2C_\Sigma} \qquad (14)$$

In addition, to get the free energy one must consider the work done by the voltage source. If one electron tunnels through the first junction the voltage source has to replace this electron, plus the change in polarization charge caused by the tunneling electron. V_1 changes according to (13) by $-e/C_\Sigma$ and hence the polarization charge is $-eC_1/C_\Sigma$. The charge q_1 gets smaller, which means that the voltage source receives polarization charge. The total charge that has to be replaced by the voltage source is therefore $-eC_2/C_\Sigma$ and the work done by the voltage source in case electrons tunnel through junction 1 and junction 2 is accordingly

$$W_1 = \frac{-n_1 e V_b C_2}{C_\Sigma}, \; W_2 = \frac{-n_2 e V_b C_1}{C_\Sigma} \qquad (15)$$

In the above classical picture, quantum mechanical effects like quantum confinement energies and changes in Fermi energy are neglected. The size of the island is assumed to be large enough for this to hold. Thus, the free energy of the complete circuit is

$$F(n_1, n_2) = E_C - W = \frac{1}{C_\Sigma}\left(\frac{1}{2}\left(C_1 C_2 V_b^2 + (ne - q_0)^2\right) + eV_b(C_1 n_2 + C_2 n_1)\right) \quad (16)$$

The change in free energy for an electron tunneling through junction 1 and 2 is given by

$$\Delta F_1^{\pm} = F(n_1 \pm 1, n_2) - F(n_1, n_2) = \frac{e}{C_\Sigma}\left(\frac{e}{2} \pm (C_2 V_b + ne - q_0)\right) \quad (17)$$

$$\Delta F_2^{\pm} = F(n_1, n_2 \pm 1) - F(n_1, n_2) = \frac{e}{C_\Sigma}\left(\frac{e}{2} \pm (C_1 V_b - ne + q_0)\right) \quad (18)$$

The probability of a tunnel event will only be high, if the change in free energy is negative - a transition to a lower energy state. The leading term in (17) and (18) causes ΔF to be positive until the magnitude of the bias voltage V_b exceeds a threshold which depends on the smaller of the two capacitances. This is the case for all possible transitions starting from an uncharged island, n=0 and q_0=0. For symmetric junctions (C_1=C_2) the condition becomes $|V_b| > e/C_\Sigma$. This suppression of tunneling for low bias is the **Coulomb blockade.** The Coulomb blockade can be visualized with an energy diagram Fig 2.

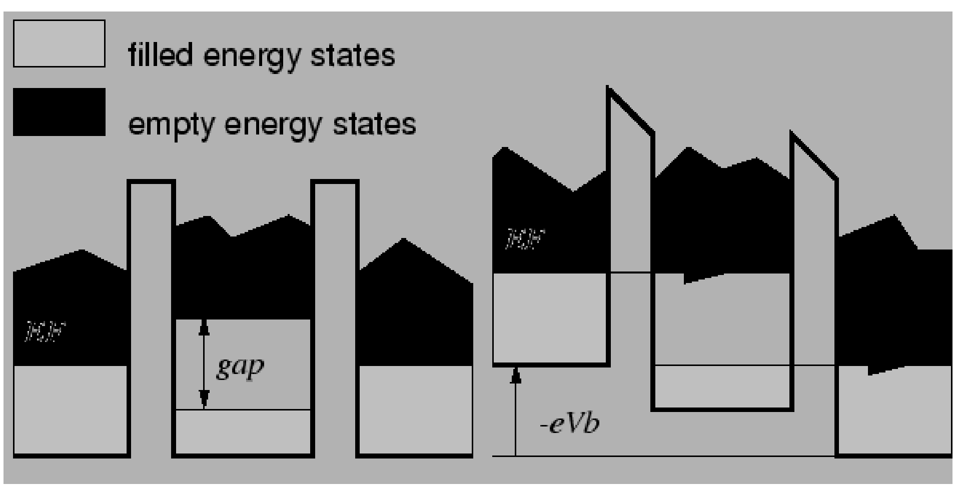
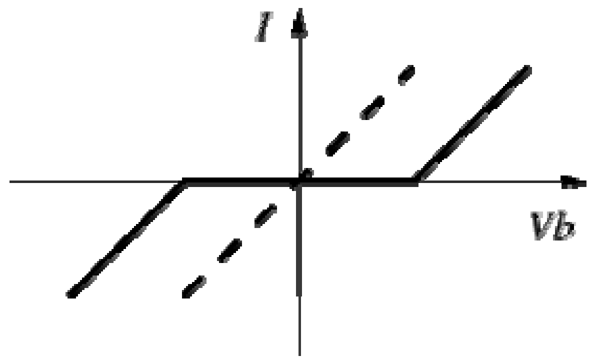


Figure 2: Energy diagram of a double tunnel junction without and with applied bias. The Coulomb blockade causes an energy gap where no electrons can tunnel through either junction. A bias larger than e/C overcomes the energy gap.

Due to the charging energy of the island, a Coulomb gap has opened. No electrons can tunnel into the island from the left or right electrode, or out of the island. Only if the bias voltage is raised above a threshold can electrons tunnel in and out, and current will flow.

However, the background charge q_0 can reduce, or for $q_0 = \pm(0.5 + m)e$ even eliminate the Coulomb blockade as shown in Fig 3 by dotted lines. This suppression of the Coulomb blockade due to virtually uncontrollable background charges is one of the major problems of single-electron devices.

Figure 3: *IV*-characteristic of a double tunnel junction. The solid line gives the characteristic for q_0=0 and the dashed line for q_0=0.5*e*. The Coulomb blockade is a direct result of the additional Coulomb energy, $e^2/2C$, which must be expended by an electron in order to tunnel into or out of the island.



If an electron enters the island via junction 1, it is energetically highly favorable for another electron to tunnel through junction 2 out of the island. Thus an electron will almost immediately exit the island after the first electron entered the island. This is a space-correlated tunneling of electrons, and establishes charge neutrality on the island. If the transparencies of the tunnel junctions are strongly different, for example $R_{T1} \ll R_{T2} = R_T$, a staircase like *IV*-characteristic appears, as shown in Fig. 4.

Carriers enter the island through the first tunnel junction and are kept from the high resistance of the second junction from immediately leaving it. Finally the carrier will, due to the high bias, tunnel out of the island, which quickly triggers another electron to enter through junction one. For most of the time the island is charged with one excess elementary charge. If the bias is increased more electrons will most of the time populate the island. If the asymmetry is turned around, the island will be de-populated and the charge on the island shows a descending staircase characteristic. Carriers are sucked away from the island through the transparent junction and can not be replenished quickly enough through the opaque one. However, the *IV*-characteristic does not change.

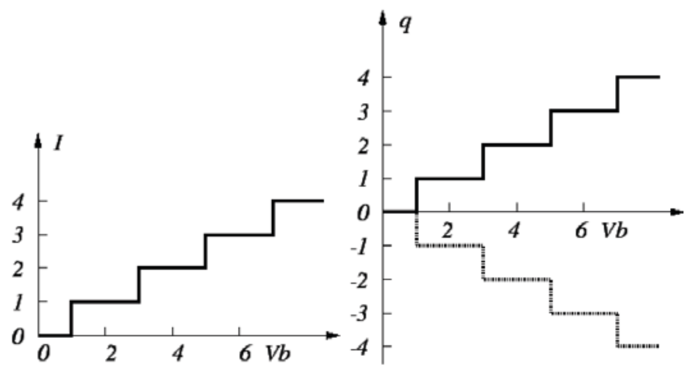


Fig 4: I-V characteristics of a double tunnel junction and charge build up with bias voltage.

4. Transport in Single Electron Transistor

Adding to the double tunnel junction a gate electrode V_g which is capacitively coupled to the island, and with which the current flow can be controlled, a so-called SET transistor is obtained.

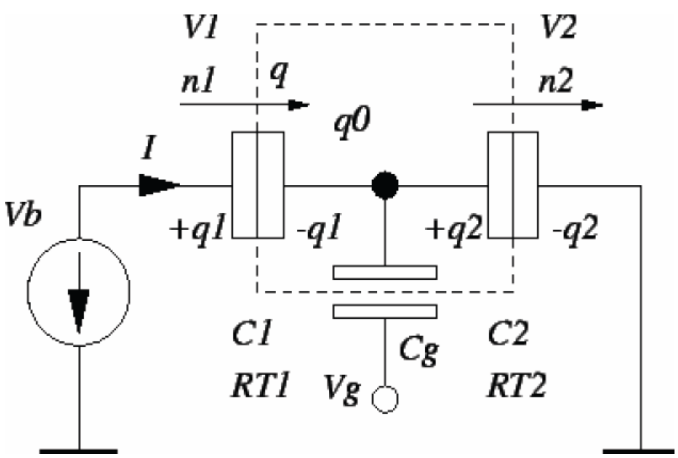


Figure 5: equivalent circuit for single electron transistor

The first experimental SET transistors were fabricated by T. Fulton and G. Dolan [6] and L. Kuzmin and K. Likharev [7] already in 1987. The effect of the gate electrode is that the background charge q_0 can be changed at will, because the gate additionally polarizes the island, so that the island charge becomes

$$q = -ne + q_0 + C_g \left(V_g - V_2 \right) \quad (19)$$

The formulas derived in the previous section for the double junction can be modified to describe the SET transistor. Substituting $q_0 \to q_0 + C_g\left(V_g - V_2\right)$ in (13), the new voltages across the junctions are

$$V_1 = \frac{\left(C_2 + C_g\right)V_b - C_g + ne - q_0}{C_\Sigma}, \quad V_2 = \frac{C_1 V_b + C_g V_g - ne + q_0}{C_\Sigma}, \quad C_\Sigma = C_1 + C_2 + C_g \tag{20}$$

The electrostatic energy has to include also the energy stored in the gate capacitor, and the work done by the gate voltage has to be accounted for in the free energy. The change in free energy after a tunnel event in junctions 1 and 2 becomes

$$\Delta F_1^{\pm} = \frac{e}{C_\Sigma}\left(\frac{e}{2} \pm \left(\left(C_2 + C_g\right)V_b - C_g V_g + ne - q_0\right)\right) \tag{21}$$

$$\Delta F_2^{\pm} = \frac{e}{C_\Sigma}\left(\frac{e}{2} \pm \left(C_1 V_b + C_g V_g - ne + q_0\right)\right) \tag{22}$$

At zero temperature only transitions with a negative change in free energy, $\Delta F_1 < 0$ or $\Delta F_2 < 0$, are allowed. These conditions may be used to generate a stability plot in the V_b-V_g plane, also referred to as "Coulomb diamonds", as shown in Fig. 6.

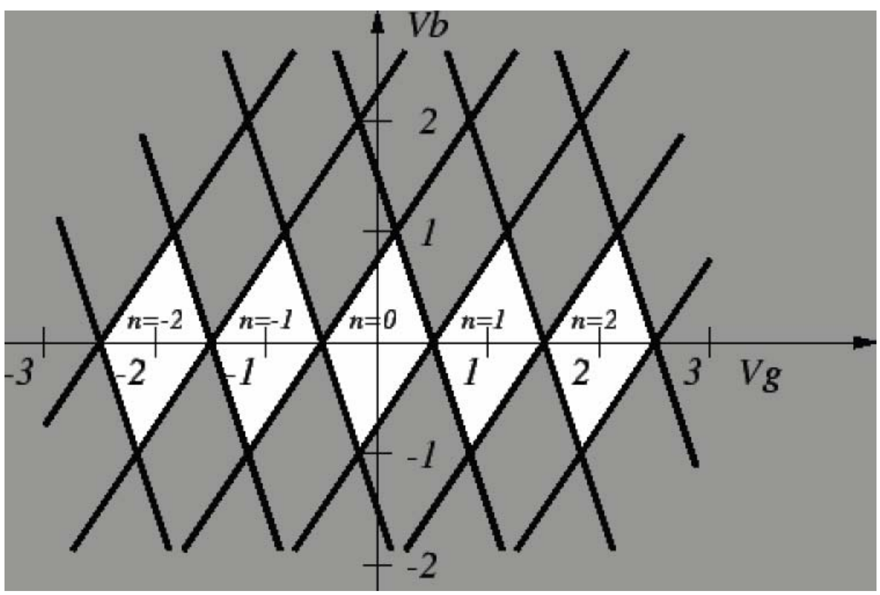


Figure 6: "Coulomb diamonds"

The shaded regions correspond to stable regions (tunnelling suppressed) with an integer number of excess electrons on the island, neglecting any non-zero background charge. If the gate voltage is increased, and the bias voltage is kept constant below the Coulomb blockade, $V_b < e/C_\Sigma$, which is equivalent to a cut through the stable regions in the stability plot, parallel to the x-axis, the current will oscillate with a period of e/C_g. These oscillations are referred to Coulomb oscillations (Fig 7 (b)).

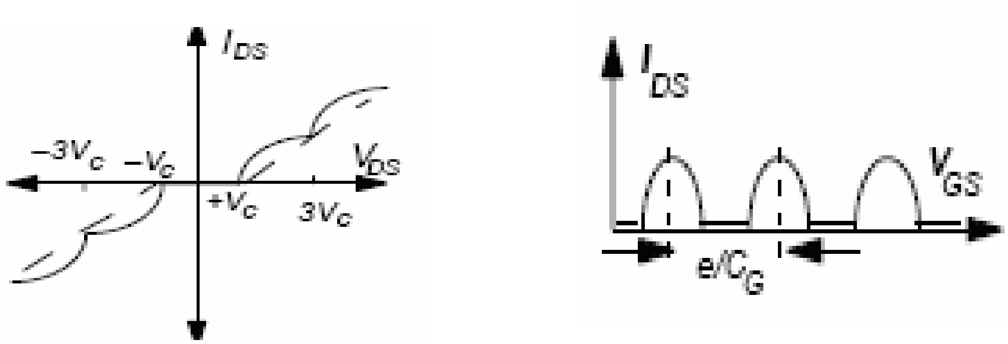


Figure 7
(a) I-V characteristics of SET **(b)** Coulomb oscillations

These oscillations have a periodicity in the applied gate voltage, where regions of suppressed tunnelling and space correlated tunnelling alternate.

If both the junctions have the same transparency to electron tunnelling, then IV characteristics are linear outside the blockade region (as shown by the dashed line in Fig.7 (a)). If the tunnel resistances are very different, the characteristics are stepped and this is known as a Coulomb staircase (as shown by the solid line in Fig 7 (a))

Thus, the charging energy may be overcome by changing the source-drain voltage as well as by changing the gate voltage [3].

5. Realization of SETs

The most common transistor in today's microchips is the metal-oxide-semiconductor field-effect transistor (MOSFET).

5.1 Problems of conventional silicon technology

Reducing the gate length and therefore the source–drain distance can lead to a “punch-through” between source and drain, when the source–drain voltage V_{SD} becomes so large that the depletion regions surrounding source and drain come

into close contact. In order to avoid transistor malfunction due to punch-through, the channel region between source and drain has to be doped higher and higher with reduced channel length. The ultimate limit for gate-thickness can be 1 nm [8]. Below this limit, direct tunnelling from the gate into the substrate becomes too large for proper transistor operation. Although the search for other gate-dielectrics opens up new perspectives for further size-reduction [9], sooner or later this problem will terminate the downscaling of MOSFET. Furthermore, by reducing the device dimensions, dopant fluctuations in the electron channel will become visible which lead to statistical shifts in the threshold voltage V_{th}. An additional problem of scaling the minimum MOS feature size below about 30 nm lies in the increasing "subthreshold current". This effect is also intrinsic to these MOS devices and causes severe problems in integrating a large number of devices while maintaining low power consumption.
Currently, several tentative technologies are investigated in order to overcome the problems arising from scaling device dimensions down to or even below 10 nm. Especially, single-electron devices such as single-electron transistors (SETs) are believed to be able to replace standard MOSFETs in this nanoscale regime. However, one main condition must be satisfied to successfully integrate single-electron devices into standard technology: the devices have to work at room temperature, which requires that their geometrical dimensions be on the order of 10 nm.

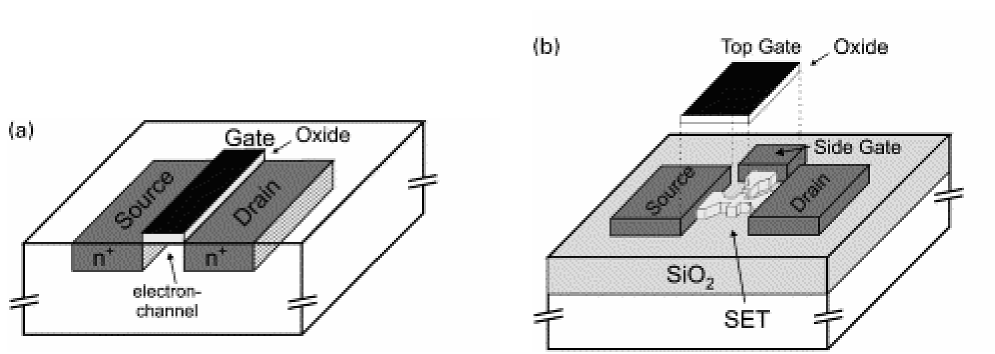


Figure 8. Comparison of the MOSFET (a) and a silicon-based single-electron transistor (b). Whereas in the conventional MOSFET a conductive electron channel is created between two highly doped source and drain regions by applying a gate voltage to a top electrode, the SET uses the charge quantization in a laterally structured electron island. In contrast to the bulk-MOSFET this kind of SET has to be fabricated out of a silicon-on-insulator film, which provides an intrinsic insulation of the electron island from the substrate.

5.2 Towards single-electron devices

In 1985 Dmitri Averin and Konstantin Likharev, then working at the University of Moscow, proposed the idea of a new three-terminal device called a single-electron tunneling (SET) transistor. Two years later Theodore Fulton and Gerald Dolan at Bell Labs in the US fabricated such a device and demonstrated how it operates [10]. The SET transistor comes in two versions that have been nicknamed "metallic" and "semiconducting", but the principle of both devices is based on the use of insulating tunnel barriers to separate conducting electrodes.

Unlike field-effect transistors, single-electron devices are based on an intrinsically quantum phenomenon: the tunnel effect. This is observed when two metallic electrodes are separated by an insulating barrier about 1 nm thick - in other words, just 10 atoms in a row. Electrons at the Fermi energy can "tunnel" through the insulator, even though in classical terms their energy would be too low to overcome the potential barrier.

Transport through such a system is dominated by the Coulomb repulsion of the electrons. For silicon, the metallic limit can be reached in practice by using a very high doping level. Since the conductance peaks are equidistant in this case, as discussed earlier in report, switching the electron island from a conducting to a non-conducting state by a proper change of gate voltage can be utilized to operate the SET.

5.3 Operation of a SET

The key point is that charge passes through the island in quantized units. For an electron to hop onto the island, its energy must equal the Coulomb energy $e^2/2C$. When both the gate and bias voltages are zero, electrons do not have enough energy to enter the island and current does not flow. As the bias voltage between the source and drain is increased, an electron can pass through the island when the energy in the system reaches the Coulomb energy. This effect is known as the Coulomb

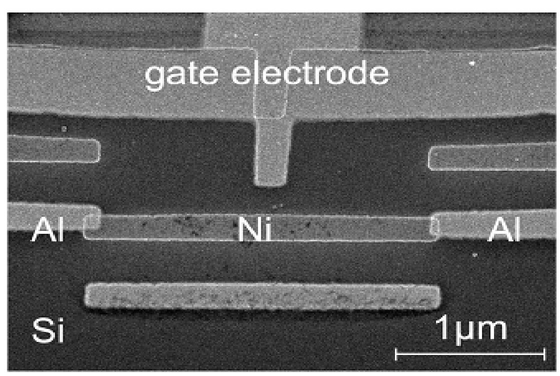


Figure 9: SEM of Al/Ni/Al SET

blockade, and the critical voltage needed to transfer an electron onto the island, equal to e/C, is called the Coulomb gap voltage.

Now imagine that the bias voltage is kept below the Coulomb gap voltage. If the gate voltage is increased, the energy of the initial system (with no electrons on the island) gradually increases, while the energy of the system with one excess electron on the island gradually decreases. At the gate voltage corresponding to the point of maximum slope on the Coulomb staircase, both of these configurations equally qualify as the lowest energy states of the system. This lifts the Coulomb blockade, allowing electrons to tunnel into and out of the island.

The Coulomb blockade is lifted when the gate capacitance is charged with exactly minus half an electron. The island is very susceptible to surrounding impurities or stray charges. In order to prevent suppress of coulomb blockade by stray charges or ions it is surrounded by insulators, which means that the charge on it must be quantized in units of *e*, but the gate is a metallic electrode connected to a plentiful supply of electrons. The charge on the gate capacitor merely represents a displacement of electrons relative to a background of positive ions.

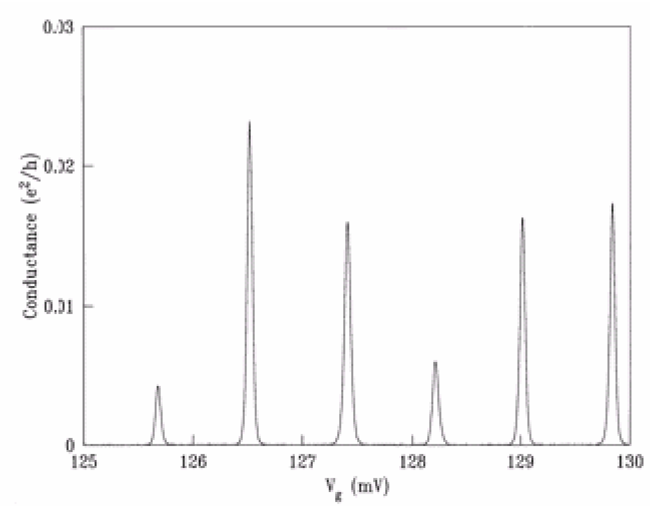


Figure 10: Coulomb oscillations in a semiconductor SET

If we further increase the gate voltage so that the gate capacitor becomes charged with -*e*, the island again has only one stable configuration separated from the next-lowest-energy states by the Coulomb energy. The Coulomb blockade is set up again, but the island now contains a single excess electron. The conductance of the SET transistor therefore oscillates between minima for gate charges that are integer multiples of *e*, and maxima for half-integer multiples of *e*.

5.4 Why use SET?

The most outstanding property of SETs is the possibility to switch the device from the insulating to the conducting state by adding only one electron to the gate electrode, whereas a common MOSFET needs about 1000–10,000 electrons. In addition, the switching time of SETs is mainly determined by the *RC*-time constants of the constrictions that can be made very small. Therefore, it is generally assumed that single-electron devices have the potential to be much faster than conventional MOSFETs. Moreover it consumes less power for operation. A major problem today is that the transistors cannot be packed very closely due to the heat they generate. Since dissipation can be highly suppressed in these novel devices, they might be especially suited for future applications in single electronics.

5.5 Towards room temperature

To integrate SET in to ICs they must be able to perform at room temperature. To observe coulomb blockade effect, one need temperature of a few hundred milli Kelvin to maintain the thermal energy of the electrons below the Coulomb energy of the device Most early devices had Coulomb energies of a few hundred microelectronvolts because they were fabricated using conventional electron-beam lithography, and the size and capacitance of the island were relatively large. For a SET transistor to work at room temperature the capacitance of the island must be less than 10^{-17} F and therefore its size must be smaller than 10 nm.

In 1998, a paper was published by Lei Zhuang and Lingjie Guo of the University of Minnesota, and Stephen Chou of Princeton University in the US that they fabricated a SET transistor in a similar way to a field-effect transistor with a channel just 16 nm wide which operates at room temperature[11]. The fabrication process generated variations in the channel that act as tunnel junctions defining several different islands, and the behaviour of the device is dominated by the smallest island. This is a step towards the realization of SETs at room temperature.

The single-island SET is sensitive to even fractional changes in the background or 'offset' charge near the island, e.g. if this changes by e/2, the Coulomb blockade may be overcome, and this is undesirable for reliable circuit operation.

A solution may be to use SETs with multiple tunnel junctions (MTJ) and islands, where the Coulomb gap is the sum of the Coulomb gaps of all the islands.
Any fluctuation in the offset charge overcomes the Coulomb blockade in only one of the islands, reducing the total Coulomb gap voltage by only a fraction. This makes the MTJ SET much less sensitive to offset charge and of greater practical significance [13].

6. Future Perspectives

6.1 Electrometry

One immediate usage of SET comes out in the form of an ideal device for high-precision electrometry. In this type of application the SET has two gate electrodes, and the bias voltage is kept close to the Coulomb blockade voltage to enhance the sensitivity of the current to changes in the gate voltage.

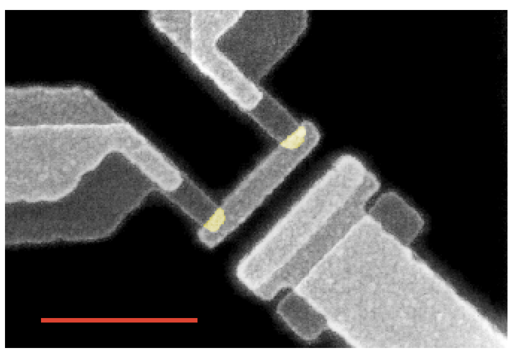


Figure 11: High precision electrometer

The voltage of the first gate is initially tuned to a point where the variation in current reaches a maximum. By adjusting the gate voltage around this point, the device can measure the charge of a capacitor-like system connected to the second gate electrode. A fraction of this measured charge is shared by the second gate capacitor, and a variation in charge of ¼*e* is enough to change the current by about half the maximum current that can flow through the transistor at the Coulomb blockade voltage. The variation in current can be as large as 10 billion electrons per second, which means that these devices can achieve a charge sensitivity that outperforms other instruments by several orders of magnitude. SET transistors have already been used in mesoscopic physics experiments that have required extreme charge sensitivity.

Recent advances in integrated circuit technology have led to a reduction in the size of electronic devices into the nanometre scale. Metal-oxide-semiconductor field effect transistors (MOSFETs) with gate lengths of a few tens of nanometres have now been fabricated, raising the possibility of large increases in the number of transistors on a chip. However, if the minimum feature size is reduced below 10 nm, quantum mechanical effects such as tunneling affect device performance significantly. The scaling-down of devices also leads to a reduction in the number of electrons available for digital switching operations. Ultimately, only a few electrons may be available for switching and statistical fluctuations in the average number of electrons would prevent the definition of clear digital states. The Coulomb blockade or single-electron charging effect, which allows for the precise control of small numbers of electrons, provides an alternative operating principle for nanometre-scale devices. In addition, the reduction in the number of electrons in a switching transition greatly reduces circuit power dissipation, raising the possibility of even higher levels of circuit integration.

6.2 Single-electron memory

Single or few-electron memory cells can use the Coulomb blockade in a SET to trap small numbers of electrons on a storage capacitor. Alternatively, the memories may be analogous to FLASH memories with the storage node reduced to the nanometer scale. In the later case, Coulomb blockade effects can also occur but are not essential for device operation. In the following, we discuss these two types of memories.

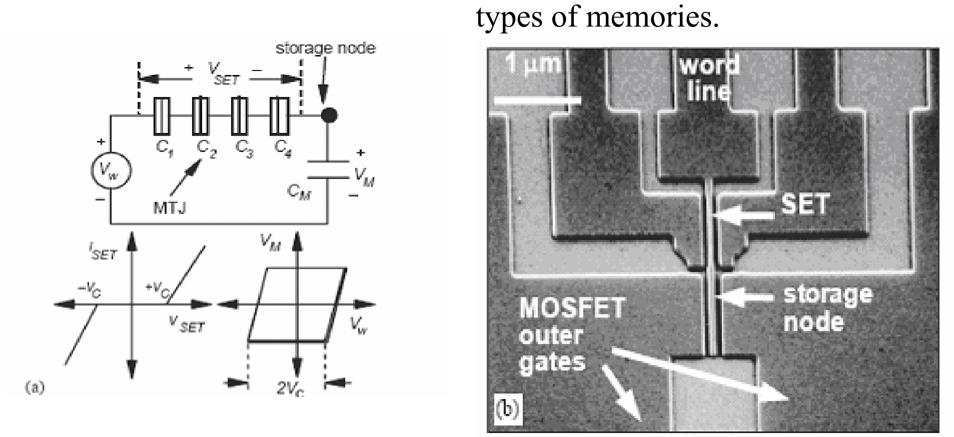


Figure12: Coulomb blockade memory using an MTJ to trap electron on a storage node.

The very low conductance within the SET Coulomb gap may be used to trap charge on a storage capacitor [12]. This type of memory often uses an MTJ (Magnetic Tunnel Junction), where the sub-Coulomb gap conductance can be lower, to control the stored charge. The operation of the memory may be understood with reference to Fig. 4(a). When the word-line voltage V_W is low, the voltage across the MTJ is within the Coulomb gap $\pm V_C$ and the MTJ does not conduct. As the word-line voltage increases and the MTJ voltage exceeds V_c charge is transferred onto the capacitor C_M, which charges up to a voltage $V_M=V_W-V_C$. If V_M is reduced, the MTJ voltage falls below V_C and C_M does not discharge. V_M remains constant until V_W is reduced to an extent that the MTJ voltage falls to $-V_C$ and the storage capacitor can discharge.

There are two different memory states, separated by the Coulomb gap $2V_c$. The number of electrons used to define the memory states is $2V_cC_M$. It is possible to scale C_M to an extent that charge corresponding to a single electron is enough to switch the MTJ into or out of Coulomb blockade.[13]. The first SET forms an MTJ trap and the gate capacitance of the second SET forms the storage capacitance. The stored charge is sensed by the source-drain current of the second SET. This type of memory has been operated with switching times down to 5 ns [14]. Few-electron memory states can also be sensed with gain using a MOSFET integrated to a SET in SOI material [14]. Here the memory states are controlled by the SET and are sensed with gain by the MOSFET. A memory cell where the memory states are separated by a few tens of electrons is shown in Fig. 4(b). The SET and the storage node are defined in the top silicon layer of the SOI material. The storage node forms the gate of a MOSFET with the channel in the substrate of the SOI material. Additional MOSFET 'outer' gates are used to create a channel in the substrate on either side of the storage node region for electrical contact to the source/drain implantation regions. The cell can operate with 10 ns long write pulses [15] and has been used to fabricate a 3×3 bit Coulomb blockade memory [16], where the memory states are separated by ~60 electrons, and the retention time is ~1 s at 40 K. The retention time of MTJ trap memories depends on the conductance within the Coulomb gap. While this is low, it can be non-zero even at low temperature due to thermally activated current and 'co-tunneling' current. The latter process involves electron transfer simultaneously across the tunnel junctions in a SET without changing the island charge. The writing time of the memory depends on the much higher conductance of the MTJ outside the Coulomb gap and can be comparatively short. Yano et al. have used their room-temperature SET design in ultra-thin polycrystalline silicon layers to develop a prototype 128 Mbit memory operating at room temperature [17]. Memory operation is based on the tunneling of single or small numbers of electrons on to storage nodes formed ‘naturally’ by isolated islands within the polycrystalline silicon layer. The write-erase times are ~10 microseconds and the retention time is up to 1 month, though this is still too low for true non-volatile operation. In contrast to MTJ-based memory cells, if the size and capacitance of the storage node in a FLASH-type memory is scaled to ~10 nm, then it can store only one or a few electrons. Here, Coulomb blockade effects can be signi0cant even at room temperature, though they are not used to control the charge. In such a ‘floating-gate’ memory, charge is transferred on to the storage node by high-field Fowler-Nordhiem tunnelling across SiO_2 or Si_3N_4 potential barriers [18,19]. The write time can be less than 1 microsecond and the retention time can be as long as 5 s at room temperature.

6.3 Single-electron logic

Since the earliest work on SETs, the possibility of logic systems using these devices has been identified [20]. The SET may be used either in a manner similar to MOSFETs to switch voltage levels, or it may be used in circuits where the presence or absence of electrons defines the ‘1’ and ‘0’ bits at specific points in the circuit. We first consider SET analogues of CMOS circuits. The oscillatory nature of the transconductance in a SET implies that it can be used to replace both the p-type and the n-type MOSFET in a CMOS circuit [21,22]. n-type MOSFETs can be replaced by SETs where the gates are biased at a point slightly before a conductance oscillation begins. Similarly, SETs biased just past the peak of a conductance oscillation are analogous to p-type MOSFETs. A two-input NAND gate using SOI SETs have been demonstrated in [23]. However, the circuit is limited by poor ‘fan-out’, noise margins and ‘offset charge’ sensitivity. Single-electron logic can also use the presence or absence of a small number of electrons at a given point in the circuit to define the ‘1’ and ‘0’ bits. Various circuits have been proposed in theory, based on transmission-line-type SET circuits or coupled-island SET circuits [24-26]. Asahi et al. [27,28] have proposed a ‘Binary decision diagram’ (BDD) logic system, where a two-way switching network is used to create logic functions and transistors with voltage gain are unnecessary. SET control circuits such as the single-electron pump [29], where clock signals transfer single or small numbers of electrons through the circuit, can be used as basic logic elements.

6.4 Carbon nanotube SETs:

Carbon nanotubes are molecules consisting exclusively of carbon that have a cylindrical form of a few nanometers in diameter and a few microns in length. The tubes can either be semiconducting or metallic, the conductivity depending on their diameter and their molecular structure. Diodes, field-effect transistors, and single electron transistors have been made from carbon nanotubes.

A single-electron transistor has been made by placing a metallic nanotube between two metal electrodes. In this case, the nanotube is the island of the SET and the contact resistances at the electrodes form the tunnel junctions of the transistor. This sort of SET has to be measured at low temperature because the charging energy is smaller than room temperature thermal fluctuations. Room temperature operation of nanotube SET's has been achieved by making two buckles in a metallic nanotube. The tube buckles much the same way as a drinking straw buckles when it is bent too far. The buckles act as tunnel barriers to electron transport and the section of the nanotube between two buckles act as the island of a single-electron transistor. The total capacitance achievable in this case is about 1 aF. In what may be the ultimate size reduction for carbon nanotube electronics, Park et al. placed a C60 molecule between electrodes spaced 1.4 nm apart. The total capacitance of the C60 molecule in this configuration was about 0.3 aF.

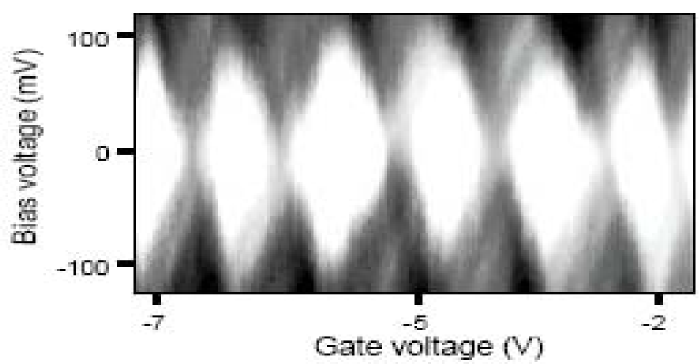


Fig 13 .Atomic force microscope image of a nanotube that is lying between platinum electrodes spaced 500 nm apart.

Fig 14. White is zero conductance in the image. The white diamonds are regions of Coulomb blockade.(T=77 K)

6.5 Nanowires:

Chemically synthesized semiconductor nanowires are attracting increasing interest as building blocks for a bottom-up approach to the fabrication of nanoscale devices and sensors. A key property of these material systems is the unique versatility in terms of geometrical dimensions and composition. Nanowires have already been grown from several semiconductor materials including structures with variable doping and composition. The nanowires has been used to make the single electron transistors at low temperatures.

Fig 16, graph of transistor from InP nanowires[31] with different length. Both traces exhibit sharp peaks corresponding to Coulomb-blockade oscillations. This clearly demonstrates that there is single-electron control over the electronic charge and the transport properties of the nanowire. The Coulomb peaks have ir regularly distributed sizes, and their *Vg*-spacing varies considerably, suggesting

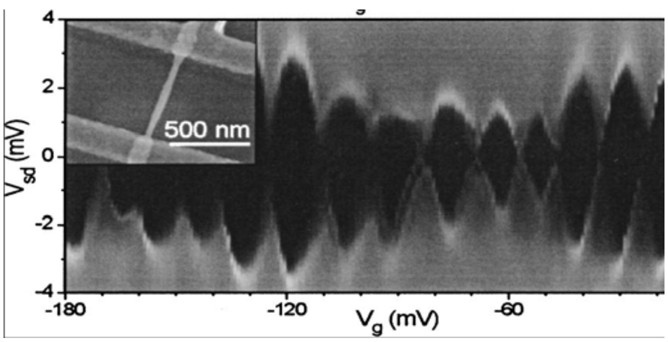


Fig 15. Gray-scale plot of differential conductance dI/dVsd versus (Vg , Vsd). dI/dVsd increases when going from dark to light gray. The measurement refers to device with length of nanowire equal to .65µm, and was taken at 0.35 K with a lock-in technique at an ac bias excitation of 20 mV. Inset: scanning electron micrograph of device C.

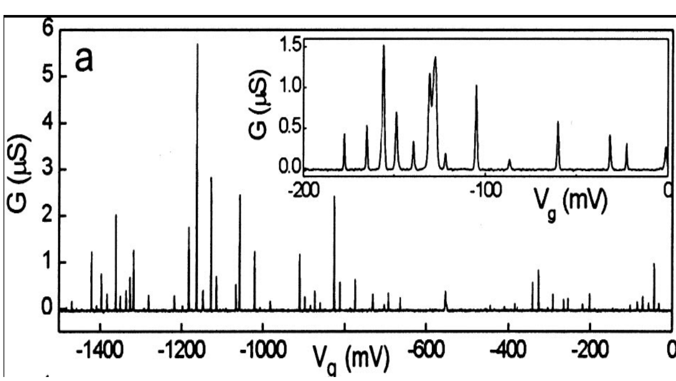


Fig 16. Conductance G versus back-gate voltage Vg measured at 0.35 K with a dc bias V_{sd}520 mV. The two traces refer to devices with different lenght.

the formation of more than one

electronic island along the nanowire. This interpretation is supported by the measurement shown in Fig. where the differential conductance *dI*/*dV*sd of device C is plotted on gray scale as a function of (*Vg* , *V*sd). In this plot, Coulomb blockade takes place within dark regions with the characteristic diamond shape. In some cases, such as for *Vg* between -40 and -90 mV, Coulomb diamonds are clearly separated from each other and have all their edges fully defined. This is characteristic of Coulomb-blockaded transport through a single electronic island. In other *Vg*-regions, however, diamonds overlap with each other, as we would expect for a nanowire containing more than one (most likely two) islands in series.
Various application of nanowires at even room temperature are known such as single-nanowire field-effect transistors (FETs), diodes, and logic gates combining both *n*-type and *p*-type nanowires. Very recently, nanowire heterostructures have been operated as resonant tunneling diodes at 4.2K.

7. Conclusion

With all the exciting properties of single electron devices, the pace of large scale integration can continue. It is not yet clear whether electronics based on individual molecules and single-electron effects will replace conventional circuits based on scaled-down versions of field-effect transistors. Only one thing is certain: if the pace of miniaturization continues unabated, the quantum properties of electrons will become crucial in determining the design of electronic devices before the end of the next decade.

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